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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/389,567	09/03/1999	JAY BRUCE ROSS	OGPT-24727	5576

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 05/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)	
09/389,567	Ross et al.	
Examiner	Group Art Unit	
Richard Ellis	2183	

--The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address--

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (Three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) Months from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on December 11, 2000.

☐ This action is FINAL

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 15-34. is/are pending in the application.

☐ Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 15-34. is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The proposed drawing correction, filed on December 11, 2000 is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119(a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2.

☒ Notice of References Cited, PTO-892

☒ Notice of Draftsperson's Patent drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

1. Claims 15-34 are presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

3. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

5. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

6. Claims 15 and 25 are rejected under 35 USC 102(b) as being clearly anticipated by Letcher, U.S. Patent 4,786,829.

Letcher taught (e.g. see figs. 1-3) the invention as claimed (as per claim 15), including a data processing ("DP") system comprising:

A) a bit stream processor (fig. 3) comprising;

B) a memory (18, col. 3 lines 35-38) having one or more inputs (X1) for receiving respective input bit streams (col. 3 lines 1-13), said input bit streams of said one or more inputs defining a plurality of input combinations to said memory (X1);

C) an opcode input of said memory (Y1) for inputting a selected one of one or more opcodes, which said selected one of said one or more opcodes operates on said input combinations (col. 3 lines 5-14); and,

D) an output of said memory for outputting an output bit stream (Y2').

7. As to claim 25, it does not teach or define above the invention claimed in claim 15 and is therefore rejected under Letcher for the same reasons set fourth in the rejection of claim 15,

supra.

8. As to claims 17 and 27, Letcher taught that the memory comprised binary memory devices which were individually and selectively read (col. 3 lines 35-38).

9. As to claims 18 and 28, Letcher taught that the input combinations comprise separate address inputs (X1) that are selected by said select one of said one or more opcodes (Y1).

10. As to claims 19 and 29, Letcher taught that the processor generated said output bit stream (Y2') at said output as a function of one or more Boolean operations performed on said input bit streams (col. 2 lines 16-23).

11. As to claims 20 and 30, Letcher taught that each said input combination of said plurality of input combinations (X1) at said one or more inputs is operated on by said opcode (Y1).

12. As to claims 22 and 32, Letcher taught that the opcode was defined by a predetermined set of Boolean operations (col. 2 lines 21-23).

13. Claims 16, 21, 23-24, 26, 31, and 33-34 are rejected under 35 USC § 103 as being unpatentable over Letcher, U.S. Patent 4,786,829, in view of Ohta et al., *New FPGA Architectures for Bit-Serial Pipeline Datapath*, Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, April 15-17, 1998.

Letcher taught the invention as detailed in the rejection of claims 15, 17-20, 22, 25, 27-30, and 32, supra. Letcher did not specifically teach that the inputs and/or results of the system were specifically single bit inputs or single bit results as recited in claims 16, 21, 23-24, 26, 31, and 33-34. Ohta et al. taught a system design for producing computational elements that were single bit computational elements (section 2, first paragraph). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have modified Letcher to accept and produce single bit results because of Ohta et al.'s teaching that designing computational elements as single bit elements produces significant time/space and speed advantages (section 2, first through fourth paragraphs).

14. As to claims 16 and 26, Ohta et al. taught that using a bit-addressable memory (fig. 12)

where input combinations (a_0 ... a_3) is mapped to a unique bit location in the memory (fig. 12, ram cell).

15. As to claims 21 and 31, Ohta et al. taught implementation of the system as a bit-serial device where the inputs accommodate single serial bit streams as detailed, supra.

16. As to claims 23 and 33, Letcher taught that the opcode was generated from a lookup table (fig. 3, 18) in accordance with a set of predetermined Boolean operations (col. 2 lines 21-23) while Ohta et al. taught advantages to implementation of the system as a bit-serial device as detailed, supra.

17. As to claims 24 and 34, Letcher taught that the finite input combinations (fig. 3, X1, Y1) were used to generated the outputs which define the opcode (Y1') while Ohta et al. the advantages of the bit-serial architecture approach as detailed, supra.

18. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

19. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

20. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone numbers for this Group are: After-final: (703) 746-7238; Official: (703) 746-7239; Non-Official/Draft: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
April 29, 2003

Richard Ellis
Primary Examiner
Art Unit 2183